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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/752,875	01/06/2004	Ronny Ronen	Intel 2207/ 979602	5346

25693 7590 11/28/2007

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EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2192	

MAIL DATE	DELIVERY MODE
11/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/752,875	RONEN ET AL.	
	Examiner	Art Unit	
	Chuck O. Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to the Application filed 09/17/07.

2. Claims 1 – 29 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 7, 9 – 14,17 – 22, 28 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Iisuka et al. USPN 5,230,050.

Regarding claim 1, a method for optimizing a number of instructions in a program file, comprising:

finding a first instruction and a second instruction in the program file that each perform a single operation and the second instruction depends on a result of the first instruction (3:15 – 25); and

forming a fused instruction that includes determining a fused opcode that represents both a first operation of the first instruction and a second operation of the second instruction (37:10 – 25).

Regarding claim 2, the method of claim 1, wherein the second instruction depends on the result of the first instruction if a destination operand of the first instruction is at least one source operand of the second instruction (37:15 – 20).

Regarding claim 3, the method of claim 1, further comprising: replacing the first instruction and the second instruction with the fused instruction in the program file after the fused instruction is formed (37:10 – 25).

Regarding claim 4, the method of claim 2, wherein the fused opcode swaps the order of applying a temporary operand, that stores the result of the first instruction, to the at least one source operand of the second instruction that is not the destination operand of the first instruction, if the second instruction is non-commutative and swaps the order of applying a first one of the at least one source operand of the second instruction to a second one of the at least one source operand of the second instruction (10:45 – 55).

Regarding claim 5, the method of claim 1, wherein forming the fused instruction includes combining at least one source operand of the first instruction and the at least one source operand of the second instruction that is not the destination operand of the first instruction to form a plurality of source operands of the fused instruction (3:30 – 40, see split or segmented into a plurality of units); and

setting a destination operand of the fused instruction to a destination operand of the second instruction (19:50 – 60).

Regarding claim 6, the method of claim 5, wherein the first instruction has two source operands and the second instruction has two source operands, and the two source operands of the first instruction are combined with a particular one of the two source operands of the second instruction that is not the destination operand of the first instruction to form three source operands of the fused instruction (19: 45 – 55, see destination segments).

Regarding claim 7, the method of claim 1, wherein the fused opcode is specified using M*N bits and the fused opcode represents one of 2.sup.M first operations fused with 2.sup.(M*N-M) second operations (32:40 – 50, equivalent resultant).

Regarding claim 9, which claims similarly as already addressed claim 1, see reasoning above.

Regarding claim 10, which claims similarly as already addressed claim 2, see reasoning above.

Regarding claim 11, which claims similarly as already addressed claim 4, see reasoning above.

Regarding claim 12, which claims similarly as already addressed claim 5, see reasoning above.

Regarding claim 13, which claims similarly as already addressed claim 6, see reasoning above.

Regarding claim 14, which claims similarly as already addressed claim 7, see reasoning above.

Regarding claim 17, the compiler version of claim 1, see rationale as previously disclosed above.

Regarding claim 18, the compiler version of claim 2, see rationale as previously disclosed above.

Regarding claim 19, the compiler version of claim 3, see rationale as previously disclosed above.

Regarding claim 20, the compiler version of claim 4, see rationale as previously disclosed above.

Regarding claim 21, the compiler version of claim 5, see rationale as previously disclosed above.

Regarding claim 22, the compiler version of claim 6, see rationale as previously disclosed above.

Regarding claim 28, the machine readable version of claim 1, see rationale as previously disclosed above.

Regarding claim 29, the machine readable version of claim 2, see rationale as previously disclosed above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 23, 24, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Djafarian et al. USPN 6,742,110 B2.

Regarding claims 23 and 26, Djafarian anticipates a processor, comprising:

a fused instruction execution unit that includes (2:30 – 37) a first arithmetic logic unit (ALU, 34) to perform a first operation (5:35 – 40) and a second ALU to perform a second operation (5:65 – 67, see D Unit ALU 38), wherein a result of the first ALU is input into the second ALU and within one clock cycle, the first ALU performs the first operation and the second ALU performs the second operation (6:1 – 20).

Regarding claims 24 and 27, Djafarian anticipates the processor of claim 23, further comprising:

an instruction fetch/decode unit that tags a fused instruction for execution on the fused instruction execution unit, if the first ALU performs a first operation of the fused

instruction and the second ALU performs a second operation of the fused instruction (2:20 – 40 also see 5:35 – 40 and 5:65 – 67 and ALU 34 and 38);

and a re-order unit, coupled to the instruction fetch/decode unit, that stores the fused instruction for retrieval by a reservation station (5:53 – 65, see A Unit register).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iisuka et al. USPN 5,230,050 as applied in claims 6 and 12, in view of Djafarian et al. USPN 6,742,110.

Regarding claims 8 and 15, Iisuka discloses all the claimed limitations as applied in claim 6 above. Iisuka doesn't expressly disclose, wherein each of the three source operands of the fused instruction and the destination operand of the fused instruction are specified using a number of bits needed to address available registers. However, Djafarian in an analogous art and similar configuration discloses the use of bit pointer registers and data registers which may be used for data flow as well ass address

generation (5:35 – 43). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Iisuka and Djafarian because, it would enable address generation data flow.

Regarding claim 16, the fused instruction of claim 12, wherein the fused opcode is specified using eight bits and each of the three source operands of the fused instruction and the destination operand of the fused instruction is specified using five bits (Djafarian, 11:11 – 12).

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iisuka et al. USPN 5,230,050 as applied in claims 6 and 12, in view of Djafarian et al. USPN 6,742,110 as applied in claim 24 and further in view of Odani et al. USPN 5,850,552.

Regarding claim 25, Iisuka as modified by Djafarian as discloses all the claimed limitations as applied in claim 24. The combination of Iisuak and Dafarian doesn't expressly discloses retrieving the fused instruction and dispatching the fused instruction to the fused instruction execution unit, if the first operation of the first ALU matches the first operation of the fused instruction and the second operation of the second ALU matches the second operation of the fused instruction. However Odani in an analogous art and similar configuration of optimizing and rearranging instructions (see abstract) discloses a replacement candidate resource means which makes combination of types of an instructions and excludes resources in combinations which do not match the combination patterns wherein the optimization apparatus obtains rearranged

instructions for the program segment from the instruction storage means. Therefore it would have been obvious to one of ordinary skills in the art at the time the invention was made to combine Iisuka and Djafarian with Odani because, it would enable rearranging the instructions for optimization more efficiently.

Conclusion

Applicant's arguments filed 09/17/07 have been fully considered but they are not persuasive.

Argument (1), on page 12, Applicant argues that the prior art doesn't disclose " 1. A program compiling method for transforming a first procedure included in a first source program into an object program...(a) compiling, when said second procedure is to be compiled into a second object program...". Applicant further argues that the cited sections in his application focus on recompilation that utilizes previous compilations.

Response (1), Applicant's plain language of claims as disclosed in claim, discloses "finding a first instruction and a second instruction in the program file that each perform a single operation and the second instruction depends on a result of the first instruction; and forming a fused instruction that includes determining a fused opcode that represents both a first operation of the first instruction and a second operation of the second instruction".

It appears that Applicant is arguing for limitations not claimed, claims doesn't call for anything pertaining to compiling or recompilation hence Applicants argument is moot.

Correspondence information

11.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

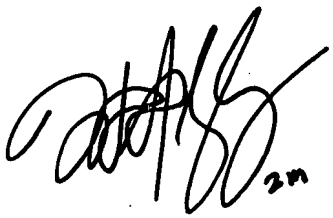
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ck.



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PRIMARY EXAMINER